Joint Zero-Forcing and Matched-Filter Processing in an Adaptive Equalizer Using the Linearly-Constrained Least Mean Square (LCLMS) Algorithm

BACKGROUND OF THE INVENTION

This invention relates to systems which utilize fractionally spaced digital equalizers to cancel the effects of channel ISI. Communication systems often employ adaptive digital equalizers to compensate for ISI introduced by unknown channel multi-path. In the demodulation process an equalizer is usually preceded by analog and digital filters in the signal-conditioning path whose purpose is to limit the noise bandwidth of the received signal. For applications involving at (T/2)-FSE the noise is reduced to a two-sided bandwidth of $2f_{sym}$. The noise-burdened signal is then sampled at $2f_{sym}$, twice the signal's Nyquist rate, whereupon a digital filter operating at $2f_{sym}$ performs further rejection of this noise. The remaining filtering task is traditionally achieved by a matched filter to minimize effects of receiver noise and ISI induced by the shaping filter. We may be tempted to bypass the matched filter and plan for the equalizer to perform both tasks, noise suppression and channel inversion. However, a FSE would perform optimal time domain zero forcing without the benefit of out-of-band noise suppression. Thus, cascading a matched filter with an equalizer filter is the standard architecture of most receivers. At the transmitter discrete samples of modulation are interpolated into an approximate continuous waveform by the pulse-shaping process. The resulting relative bandwidth reduction confines the vast majority the signal's spectral energy to frequencies below the maximum transition band frequency. Because of this, the vast majority of ISI distortion occurs for frequencies ranging from DC to the edge of the shaped signal's transition band. Hence, the majority of inverse channel modeling performed by the FSE occurs up to the maximum edge of the signal's transition band. Beyond this frequency we attempt to reform the digital equalizer into a MF by controlling the spectral sidelobes, and in so doing, the RRC MF which normally precedes the equalizer is eliminated.

SUMMARY OF THE INVENTION

The present invention demonstrates that through constrained optimization a fractionally spaced digital equalizer can perform both ISI cancellation and MF processing. In high data rate applications the advantage in forming a joint ZF-MF FSE is that the FPGA multipliers of the MF can be time-shared with those used for ZF so as to conserve FPGA real estate in a digital receiver. That is, a time-division scheme allows both the equalization and MF processes to access a single bank of multipliers rather than having two separate banks for each. In low data rate applications a single multiplier may service the entire workload of the receiver. Here, the advantage of a joint ZF-MF is the conservation of ROM memory since the RRC coefficients are generated within the FSE adaptively rather than being accessed from memory.

The scope of this application need not be specific to the world of communication theory. Any applications which utilize digital equalizers operating above the Nyquist rate and are preceded by a filter also operating above the Nyquist rate may make use of the LCLMS update to manifest a joint update.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a subset of the standard communications link.

FIG. 2, *the proposed patent in terms of the **decision-directed embodiment**,* is block diagram of the time-multi-plexing scheme of the FS-LC-LMS-DDE equalizer.

FIG. 3 defines an algorithm to control the rate of acquisition of the decision-directed equalizer embodiment.

FIG. 4 defines an algorithm to control acquisition and parameters of the constrained update.

FIG. 5, *the proposed patent in terms of the **decision-feedback embodiment**,* is block diagram of the time-multi-plexing scheme of the FS-LC-LMS-DFE equalizer.

FIG. 6, *the proposed patent in terms of the **blind-constant modulus embodiment**,* is block diagram of the time-multi-plexing scheme of the FS-BCM-E equalizer.

DETAILED DESCRIPTION OF THE INVENTION

In this embodiment we consider the joint ZF-MF digital equalizer as applied to a digital communication system. As illustrated in Figure 1 informational bits are modulated to discrete levels of complex 2-tuples via constellation mapping **1**. The square-root-raised cosine pulse-shaping filter **2** interpolates the discrete levels of modulation providing for bandwidth reduction. The transmitted signal may encounter channel multi-path **3** and/or additive white Gaussian noise (AWGN) **4**, or other possible sources of interference such as CW jamming, all of which cause distortion. After passing through a receiver's signal conditioning the distorted signal is filtered with RRC MF **5** designed to (1), suppress AWGN band-limited by the signal conditioning and possible adjacent channel interference and (2), restore full SNR with respect to ISI distortion introduced by the transmitters RRC shaping process. The distorted

update (LC-LMS-DDE). The equalized data is formed from the inner product of the input data and the weights of the equalizer, and the weights are obtained by an LMS based gradient descent. The first constraint of the dual constraint update is the standard minimization of the difference between the input and output of the decision circuit. The second constraint, that of the MF, is driven by minimizing the difference between a scalar constraint level parameter β and a 2nd inner product, that between the weights and samples of the constraint sinusoid accessed at equalizer output sample n. The addition of the 2nd constraint transforms the LMS update to the LC-LMS recursion.

Specifically, with respect Figure 2 the LC-LMS-DDE update consists of two banks of delay registers, a register bank **10** to store the input data to be equalized, and a register bank **11** to store the contents of a complex constraint sinusoid. At time $t1$, an instant after the last sample of a set of FS input samples enters the data register bank, switch T1 **12** is closed to allow the register bank to engage the FSE's weights **13** to form the inner product. The equalized estimate is formed from an array of summing elements **14** used to sum the inner product and is passed into a decision device called a slicer **15** which quantizes the estimate to the constellation region it resides in. A summing node **16** is used to form the difference between slicer input and output called the decision error. In turn, the decision error is complex conjugated and used to drive the FSE weights according an adjustment parameter defined in ALG-1 **17**. ALG-1 refers to one of any number of algorithms which control the rate of acquisition of the adaptive system. In many cases this parameter is a scalar μ such that $0 < \mu < \mu_{max}$, and μ_{max} is inversely proportional to the signal energy input to the FSE. Hence, one particular embodiment for ALG-1 is shown in Figure 3 involving a complex conjugation operator **18**, an adaptation constant μ. **19**, and a multiplier **20**.

The constraint register bank **11** spans the duration of the data register bank and stores samples of a complex sinusoid that is to be made orthogonal to the FSE by the LC-LMS update at its center frequency. At time $t2$, an instant after $t1$ but prior to the next successive input set of fractionally spaced data samples, switch T1 is opened and switch T2 **21** is closed to allow computation of a second inner product between the contents of the complex constraint register bank and the FSE weights. Once again the array of summers **14** computes the sum of the inner product, and the resulting scalar is compared to the constraint threshold β **22** using the summing node **16**. The difference is driven to minimization by ALG-2 **23**. As shown in Figure 4 the constraint error is passed through ALG-2's complex conjugation operator **24** and is passed on to a multiplier **25** which computes its product with a constraint dependent scalar **26**. This scalar is dependent upon which out-of-band frequency is being accessed at the current update equalizer output sample n. The index is formed from a FSE output sample counter and modulo-addition. First, the sample counter n **27** is subtracted by 1 **28** using an adding device **29**. A modulo-N operator **30** divides by N and returns the remainder which is added back to 1. As n increses the resulting number cyclically repeats between 1 and N and indexes an array **31** storing the N out-of-band frequencies. The frequency is passed to a sinusoidal generator **32** which creates the samples of the complex constraint sinusoids. If i represents the indice into the frequency array then $\underline{c}(i)$ is generated and forms the scalar $1/\ \underline{c}^H(i)\underline{c}(i)$. The complex constraint sinusoids are loaded into the constraint register delay bank at the equalizer's output rate, or equivalently, the symbol rate. The LC-LMS algorithm repeats with the next successive pair of data samples input to the data register delay bank.

The preceding architecture also refers to other digital equalizer embodiments such as the *decision-feedback equalizer* (DFE) as shown in Figure 5. The same components comprising the LC-LMS-DDE are also present for the LC-LMS-DFE with the exception of the following. A bank of M delay registers **33** stores the previous M decisions from the slicer output and weights them according to the values of the DF weights **34** to form an inner product. Again a bank of summing elements **35** computes the sum of the inner product. This sum is added to the sum of the inner product in the T1 switch path to form the equalized estimate. After it has been conjugated the decision error is passed through ALG-3 **36**. As shown in Figure 6, ALG-3 consists of a complex conjugate operator **37**, a multiplier **38**, and an adaptation constant **39** to control the rate of DF acquistion. The adaptation constant **39** may or may not take on the same value as the adaptation in ALG-1.

Other equalizer embodiments that reside within the scope of this the patent of constrained optimization are the *fractionally-spaced lattice equalizer* (FS-LATTICE-DDE) Figure 7 and *fractionally-spaced lattice-feedback equalizer* (FS-LATTICE-DFE) Figure 8 (NOT FINISHED YET).

Another embodiment pertains to the statistically-based *fractionally-spaced blind equalizer* and *fractionally-spaced blind-feedback equalizer* For the purposes of illustration within this patent the blind equalizer under the supervision of the constant modulus algorithm is studied; the *fractionally-spaced blind constant modulus* equalizer (FS-BCM-E, FS-BCM-DFE) as shown in Figures 10 and 11.

Although a particular embodiment of the invention has been described in detail for purposes of illustration, various modifications and enhancements may be made without departing from the spirit and scope of the invention